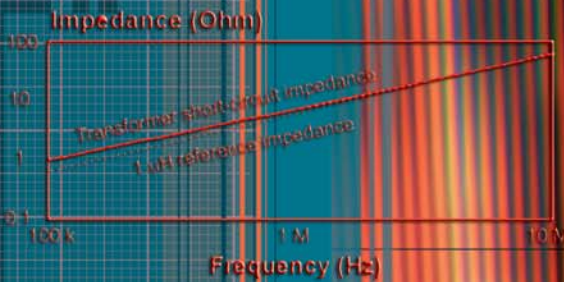
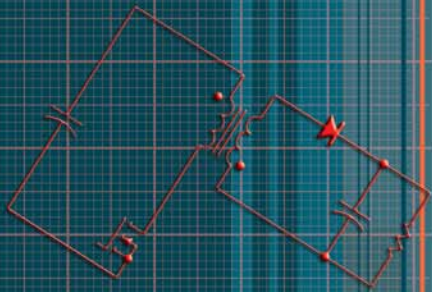


Flyback Converter Snubber Design



by Dr. Ray Ridley



In this issue, and previous issues of SPM, we cover the latest technologies in exotic high-density power. Most power supplies in the commercial world, however, are built with the bread-and-butter technologies we have used for decades. Square wave PWM converters are still the most cost effective way to provide regulated voltages in electronics systems, and will remain so for many years to come.

All PWM converters have nonideal parasitics that lead to ringing waveforms that must be properly suppressed. Without this, semiconductors can be prone to failure, and noise levels will be higher than necessary. In this article, we will talk about practical design techniques for the most commonly used snubber and clamp circuits for the flyback converter.

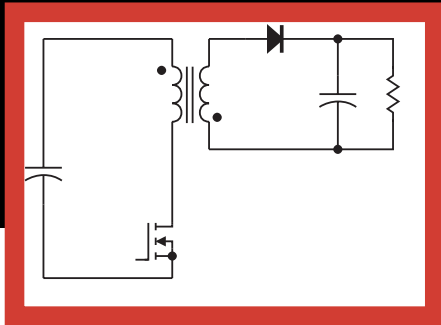


Figure 1a: Flyback converter schematic

Flyback Converter with No Snubbers

Figure 1a shows the basic flyback circuit with no snubbers in place. Ideally, the circuit has squarewave characteristics when turning on and off. In practice, however, the turn-off of the power switch interrupts current through the leakage inductance of the transformer, that this will cause a voltage spike on the drain of the FET.

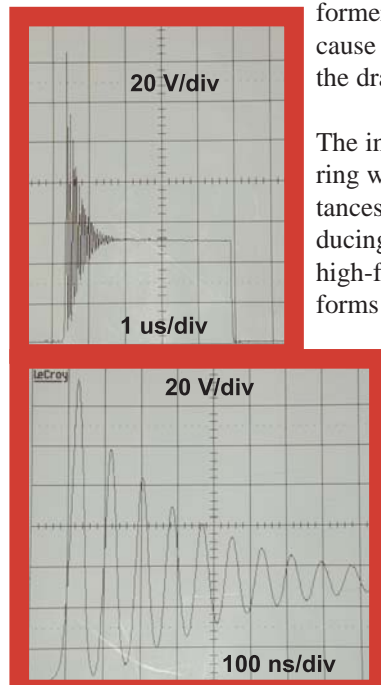


Figure 1b: Flyback converter drain voltage with no snubber

The inductance will then ring with stray capacitances in the circuit, producing large amplitude high-frequency waveforms as shown in Figure 1b. On the flyback primary, the measured leakage inductance rings with primary capacitances.

Many application notes and designs ignore the ringing waveforms and operate the converter without addressing the issue. There are two problems with this: firstly, there is excessive voltage on the drain of the FET which can lead to avalanche breakdown and eventually failure of the device. Secondly, the ringing energy will be radiated and conducted throughout the power supply, load, and electronic system, creating noise issues and even logic errors. The ringing frequency will also show up as a peak of the EMI spectrum in both radiated and conducted EMI.

In most designs, this is not acceptable, and it is necessary to add circuit elements to damp the ringing (using RC snubber), or clamp the voltage (with RCD clamps), or both. The design of these networks is a combination of measurements and analysis to ensure a rugged and dependable result. In this article, we will review the two different types of snubber design procedures.

Primary RC Snubber for Flyback Converter

Figure 2a shows an RC snubber circuit, used to damp the ringing on the drain of the FET. The resistor provides damping for the LC resonance of the power circuit, and the series capacitor prevents the voltages at the power stage switching frequency from being applied across the resistor. The capacitor is sized to allow the resistor to be effective at the ringing frequency. The RC snubber is best placed directly across the semiconductor that is to be protected.

If you are using a current sense resistor in series with the FET, make sure that the snubber is connected to the top of the sense resistor, not to ground. When you do this, the sense resistor will not see the current spike at turn-on when the snubber capacitor is discharged.

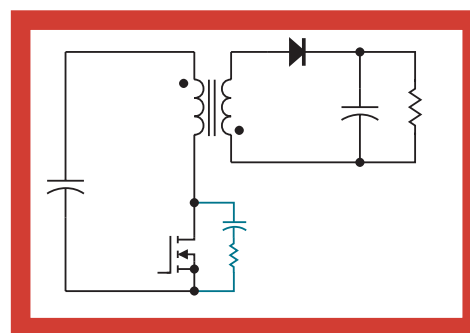


Figure 2a: Flyback converter with primary RC snubber. Ringing frequency = 12 MHz.

The requirements of designing the RC snubber are simple—choose a resistor to properly damp the ringing, select a capacitor, and make sure that the dissipation of the network is not excessive. In the days of low-frequency switching, it was not uncommon for engineers to use resistor and capacitor decade boxes to empirically try different values to damp the ringing. We prefer a more analytical approach than this to optimize the design. Decade boxes don't work that well with ringing frequencies well above 1 MHz, and this was never an effective method for finding the best compromise of dissipation and damping.

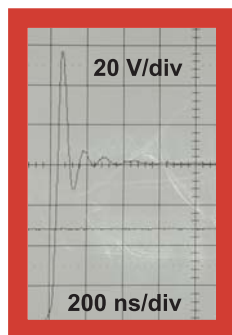


Figure 2b: Flyback converter drain waveform with primary RC snubber added

Design Step 1: Measure Leakage Inductance

The first step in the design of an effective RC snubber is to measure one of the parasitic elements causing the observed ringing. There are two choices of components to measure— the total effective capacitance, or the leakage inductance. Capacitance is hard to define and measure. It is a combination of nonlinear semiconductor junction capacitances, transformer winding capacitance, and any other stray capacitances such as heatsinks. The ringing frequency is often high enough that even an oscilloscope probe can impact the waveforms when connected to the circuit.

NOTE: Whatever you do, do not guess at the value of the leakage inductance. It is a common, (and very flawed), rule of thumb to assume that the leakage inductance is 1% of magnetizing inductance. It can be more than an order of magnitude different from this, and snubber design based on the 1% number will rarely be useful.

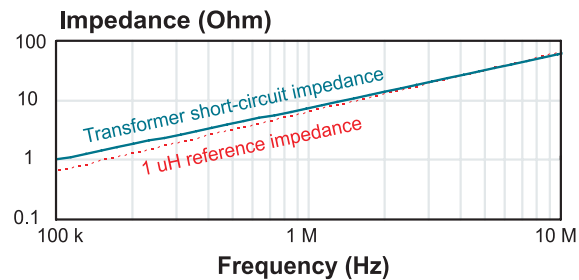


Figure 3a: Flyback transformer impedance measurement with secondary shorted

That leaves us with the leakage inductance of the transformer, L , which is easy to measure with a frequency response analyzer. To do so, a short circuit is applied across the secondary (or secondaries) of the flyback transformer, and the impedance is measured from the primary winding. It is recommended to do this across a wide range of frequencies, including the power supply switching frequency, and the snubber ringing frequency, in order to capture the proper value of leakage inductance.

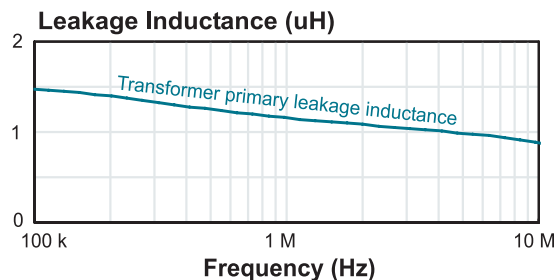


Figure 3b: Flyback transformer primary leakage inductance measurement

Due to proximity effects in the transformer, the leakage inductance can vary significantly at higher frequencies, as shown in Fig. 3b. Notice that the leakage actually drops with frequency. For the design of the primary RC snubber, we use the value of inductance obtained at 12 MHz.

Design Step 2: Measure the Snubber Ringing Frequency

Fig. 1b shows the undamped ringing on the drain of the FET. As mentioned before, care must be taken in capturing this waveform. You can usually see it without even touching the drain of the FET with the scope probe, and this gives the most accurate measurement unaffected by the probe capacitance.

Notice that the ringing on the FET is asymmetrical, with sharp peaks, and wider bottoms of the waveforms. This is due to the nonlinear nature of the output capacitance of the FET, which reduces as the voltage is increased. From this waveform, estimate the ringing frequency, f_r . To proceed with a good snubber design, this frequency should preferably be two orders of magnitude higher than the switching frequency, or dissipation will become excessive. If this is not the case in your power supply design, you must work on reducing the leakage inductance of the transformer, or the circuit capacitance, or both.

Design Step 3:

Calculate the Snubber Resistor and Capacitor

In order to damp the ringing properly, we need to calculate the characteristic impedance of the resonant circuit. This is given by:

$$Z = 2\pi f_r L$$

The ringing will be well damped if we use a snubber resistor equal to the characteristic impedance of the ringing. We therefore use the design point of $R=Z$ to select the resistor.

The snubber capacitor is used to minimize dissipation at the switching frequency, while allowing the resistor to be effective at the ringing frequency. The best design point to start with is the impedance of the capacitor at the ringing frequency equal to the resistor value.

$$C = \frac{1}{2\pi f_r R}$$

Design Step 4:

Calculate the Snubber Dissipation

The dissipation is determined by the size of the snubber capacitor. The approximate dissipation is given by:

$$P_{sn} = CV^2 f_s$$

where V is the voltage on the FET given by the input voltage plus the reflected output voltage. Make sure to use the switching frequency, f_s , in this calculation, not the ringing frequency.

Note: the usual factor of $\frac{1}{2}$ does not appear in this expression since the resistor will dissipate power both when the capacitor is charged and discharged. The

charging is done with the inductance, and as such, the dissipation may be a little lower than predicted by this expression. However, it is a good conservative design estimate.

Design Step 5:

Experimental Verification of Design

The final step in the design is to experimentally test the snubber. Do not skip this important step. Errors in measurement, miscalculation, excessive lead lengths and nonlinear circuit events during switch transition can all affect how well the snubber will work.

Figure 2b shows the ringing on the drain of the primary FET with the snubber in place. Notice that the ringing is very quickly damped out, greatly reducing EMI. The peak of the waveform is also substantially reduced. The snubbed waveform is shown with an input of 50 V, whereas the unsnubbed waveform was at 30 V input.

It is difficult to reduce this voltage spike much further using just a simple RC snubber. For many applications, the RC snubber is the best solution, but for some offline solutions using integrated power controllers, it is necessary to clamp this voltage to a lower value to prevent failure of the FET. This is discussed in the next section of this article.

Primary RCD Clamp for Flyback Converter

Figure 4a shows an RCD clamp circuit, used to limit the peak voltage on the drain of the FET when an RC snubber is insufficient to prevent switch overvoltage. The RCD clamp works by absorbing the current in the leakage inductor once the drain voltage exceeds the clamp capacitor voltage. The use of a relatively large capacitor keeps the voltage constant over a switching cycle.

The resistor of the RCD clamp always dissipates power, even when there is no power in the main converter. Even with very little load on the converter, the capacitor will always be charged up to the voltage reflected from the secondary of the converter, v_f . As the load is increased, more energy will flow into the capacitor, and the voltage will rise by an additional amount, v_x , above the ideal square wave flyback voltage. The voltages are defined in Figure 4a.

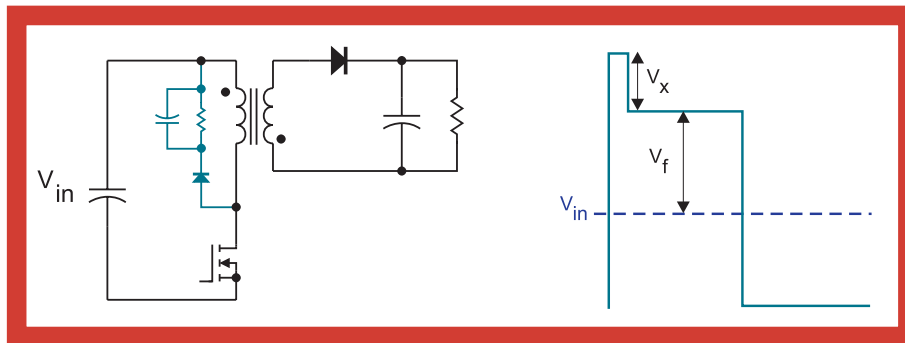


Figure 4a: Flyback converter with primary RCD clamp

$$P_{sn}^{max} = P_l \left(1 + \frac{v_f}{v_x^{max}} \right)$$

In other words, the higher we let the clamp voltage rise on the switch, the lower the overall dissipation. But of course, we must balance this against the total

dissipation seen across the power FET, so we cannot arbitrarily reduce dissipation.

Design Step 1: Measure Leakage Inductance

It is crucial to measure the leakage inductance of the flyback transformer prior to designing the snubber. Details of how to do this are given earlier in this article for the RC snubber design. For the RCD clamp, we are concerned with how much energy is stored in the leakage inductance, rather than the incremental leakage value at the ringing frequency. For a more conservative design, it is better to use the value of leakage inductance measured at the switching frequency, rather than the ringing frequency.

We'll iterate again - don't guess at the leakage inductance, or use the 1% rule for its value. Measure it to be sure of a good snubber design.

Design Step 2: Determine Peak Clamp Voltage

Now you must decide how much voltage can be tolerated on the power MOSFET, and calculate the amount of power that will be dissipated in the clamp with this clamp level. The energy stored in the leakage inductance, L , with a current I_p at turn-off is given by:

$$P_l = \frac{1}{2} LI_p^2 f_s$$

Analysis of the RCD snubber has appeared in papers and numerous application notes. It is assumed that there are no stray capacitances to charge, and that all the leakage energy is conducted into the snubber capacitor from the leakage inductance. The capacitor is assumed to be large enough that its value does not change significantly during one switching cycle.

With these assumptions, the power dissipated by the RCD clamp can be expressed in terms of the energy stored in the inductor as follows:

A typical design is for the voltage v_x to be equal to $\frac{1}{2}$ the flyback voltage. In this case, the dissipation is equal to 3 times the stored energy in the leakage inductance. This is a conservative estimate, however. It does not account for lossy discharge of the inductor, nor for stray capacitance. In reality, the design will have less loss in the clamp than anticipated due to these effects.

For high-voltage offline designs which are often constrained to use a FET with a maximum voltage of 600 or 650 V, the voltage v_x will have a hard limit set by the maximum input line, maximum current, and FET breakdown voltage. Do not exceed the stated V_{ds} of the FET, and be aware that the breakdown degrades with temperature. Some designers rely on the avalanche capability of the FET to let them regularly exceed the breakdown voltage. We do not recommend this approach for a rugged power supply.

Design Step 3: Select Clamp Resistor

The capacitor of the snubber needs to be large enough to keep a constant voltage while absorbing the leakage energy. Apart from this consideration, its value is not critical, and will not affect the peak voltage when the snubber is working properly.

The resistor is the element that is crucial in determining the peak voltage v_x , and it should be selected with:

$$R = \frac{2v_x T_s (v_f + v_x^{max})}{LI_p^2}$$

A larger value of resistor will slow the discharge of the clamp capacitor, and allow the voltage to rise to a higher value. A smaller value will result in a lower clamp voltage, but the dissipation will be increased.

In most designs, the clamp resistor value obtained will be very different from the resistor value for the RC snubber described earlier. Don't expect to get similar values.

Design Step 4: Calculate Power Loss

The snubber design is now complete, but we need to know what the dissipation will be for currents other than the maximum current. Use the following equation to calculate the voltage rise in a known snubber for a given peak current and leakage inductance.

The value of the voltage rise, v_x , above the flyback voltage is given by:

$$v_x = \frac{1}{2} \left(\sqrt{v_f^2 + 2 \frac{LI_p^2 R}{T_s}} - v_f \right)$$

and the power dissipation is given by:

$$P_{sn} = \frac{(v_x + v_f)^2}{R}$$

Design Step 5: Experimental Verification

As with the design of the RC snubber, experimental verification of the design is essential. Figure 4b shows the effectiveness of the circuit in clamping the peak value of the FET drain voltage.

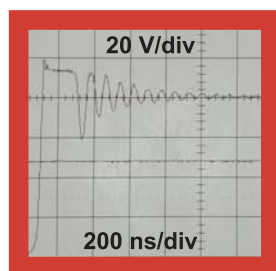


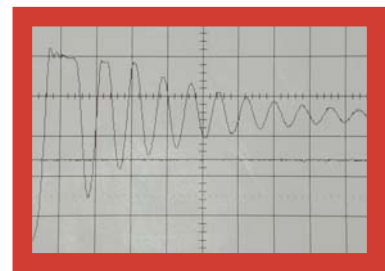
Figure 4b: Flyback converter MOSFET voltage with primary RCD clamp

This figure also shows a limitation of the RCD clamp. After the clamping period is finished, the circuit resumes ringing. With ideal components, this would not happen. However, the diode of the RCD clamp has a finite reverse recovery time which allows the leakage inductor current to flow in the opposite direction in the

diode, resulting in ringing. The type of diode chosen for the RCD snubber is crucial. It must be as fast as possible with the proper voltage rating.

The severity of this ringing will depend on the the reverse applied voltage across the RCD diode. The higher you allow the clamp voltage to climb, the lower the dissipation, but the more voltage and dv/dt is applied to the diode. A mere 20 ns turn-off delay is a substantial portion of the ringing waveform period. Figure 4c shows how this ringing is increased as the allowed clamp voltage is raised. While the FET is still well protected, the RCD snubber in this case has not solved the EMI problem of the ringing waveform.

Figure 4c: Flyback converter MOSFET voltage with primary RCD clamp and decreased dissipation (ie increased value for v_x)



The ringing can subsequently be damped out again by reintroducing the RC snubber, designed as described above. Figure 4d shows the drain waveform with both an RCD clamp and RC snubber in place. This provides the best protection for the FET, and the lowest EMI signature, but results in the highest power dissipation.

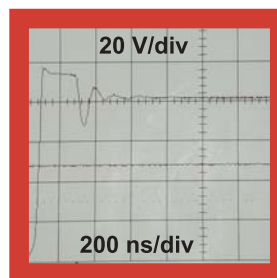


Figure 4d: Flyback converter MOSFET voltage with primary RCD clamp and RC snubber

Secondary RC Snubber for Flyback Converter

Many designers spend time in designing effective snubber for the primary of their circuit in order to protect the main power switch. Once the design is complete, the waveforms look clean on the primary side, and another source of noise and stress is often overlooked.

If a probe is placed on the secondary side of the power transformer, another ringing waveform is observed due to the turn-off of the output power diode. Figure 5b shows this waveform with two different time scales. The excess voltage applied across the output rectifier is severe, and is often even more destructive than the primary waveforms. Schottky rectifiers, especially, are very unforgiving of excessive voltage, and these ringing waveforms must be suppressed in a similar way to the primary waveforms.

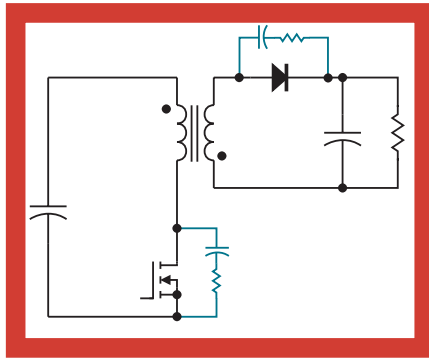


Figure 5a: RC snubber added to the flyback secondary

The secondary snubber is best placed directly across the diode. The design procedure for the secondary snubber is almost identical to the primary snubber. Make sure that you use the right value of leakage, calculated from the measured primary inductance divided by the turns ratio squared.

Notice that the waveform is more noticeably asymmetrical than the primary waveforms. The secondary capacitance is dominated by the diode capacitance, and the transformer only makes a small contribution. Hence the nonlinearity of the semiconductor capacitance is more clearly seen.

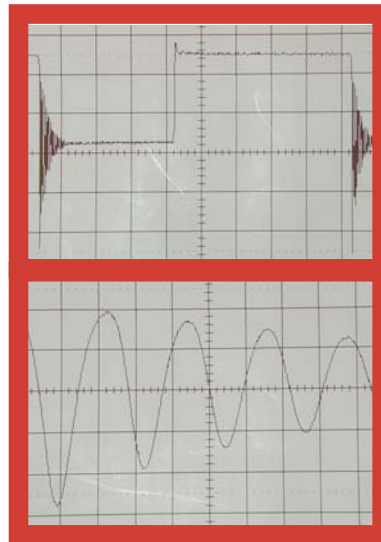


Figure 5b: Secondary diode waveform without snubber. Ringing frequency = 24 MHz

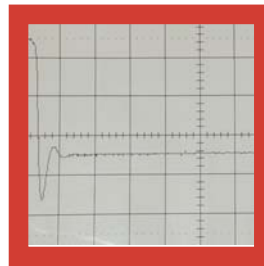


Figure 5c: Secondary diode waveform with snubber

You can also see that the secondary ringing frequency is much higher than the primary ringing frequency, 24 MHz versus 12 MHz. This is good since it makes the secondary waveform much easier to snub with minimal dissipation. The higher the ringing frequency relative to the switching frequency, the better.

Figure 5c shows the result of the RC snubber applied to the secondary. The waveform is very effectively damped with less than 100 mW of dissipation (for a 24 W output).

Don't forget the auxiliary outputs of your converter, too. Each secondary diode will need an RC snubber applied to properly protect the device.